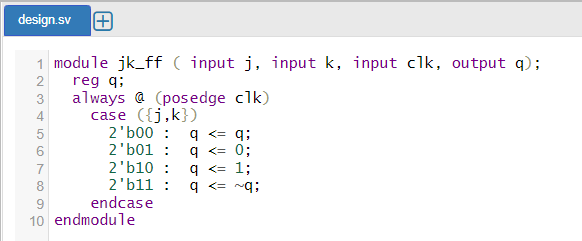
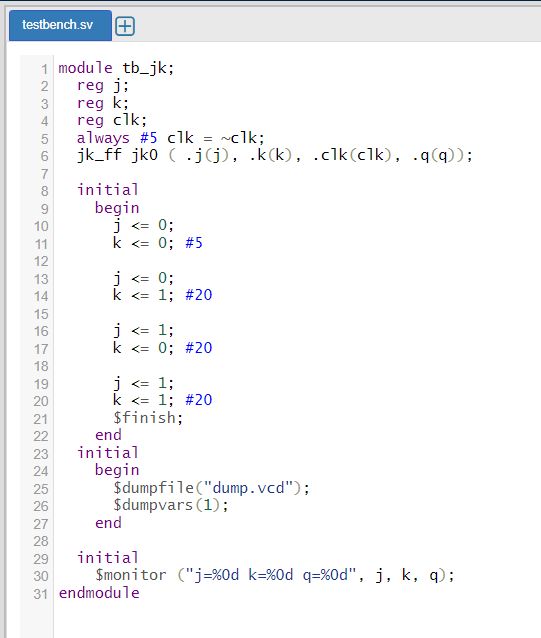
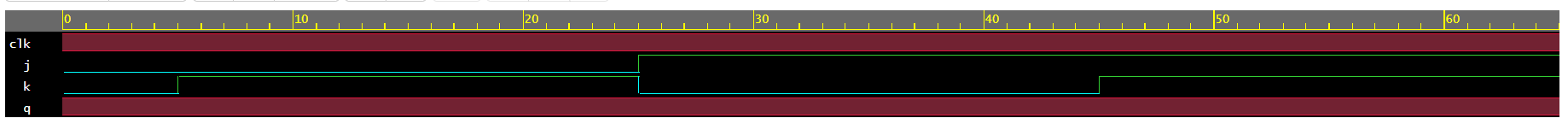
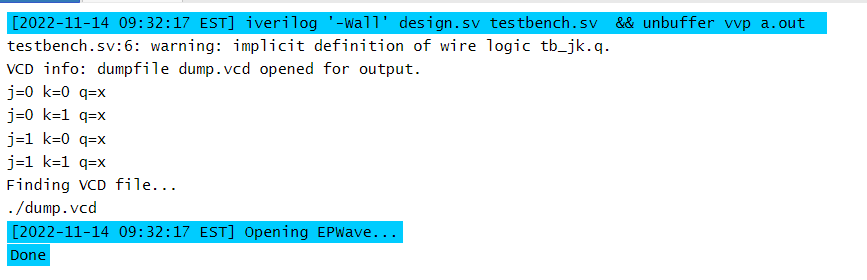
**LAB 9: Flip Flops (JK, D, T)**

**Question 1: Write a Verilog code to implement J-K flip flop and validate the code via a suitable Test bench code.**

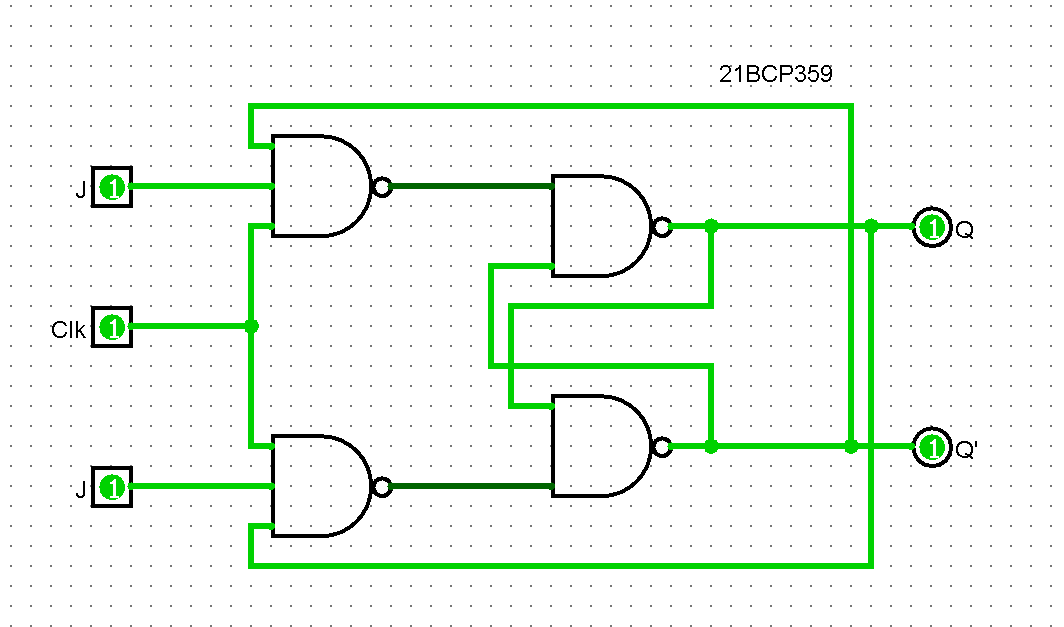
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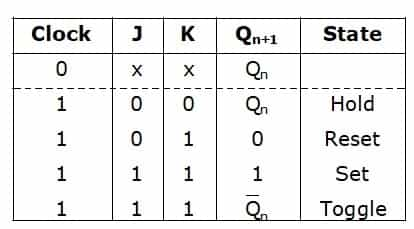
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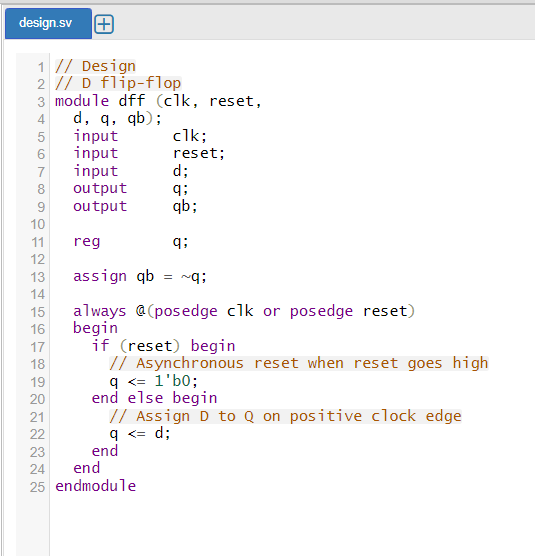
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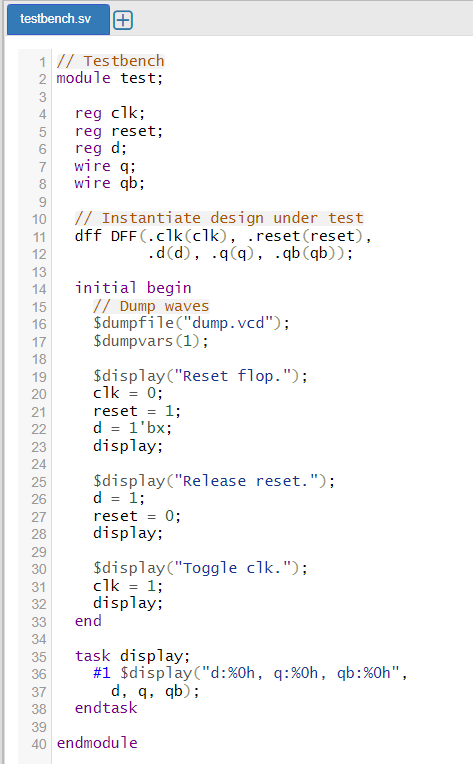
**Question 2: Design a J-K flip flop in Logisim and validate the circuit.**

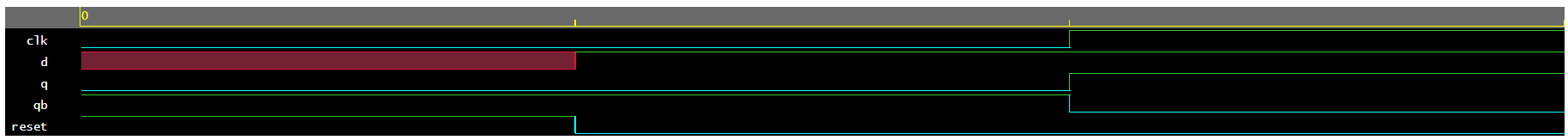
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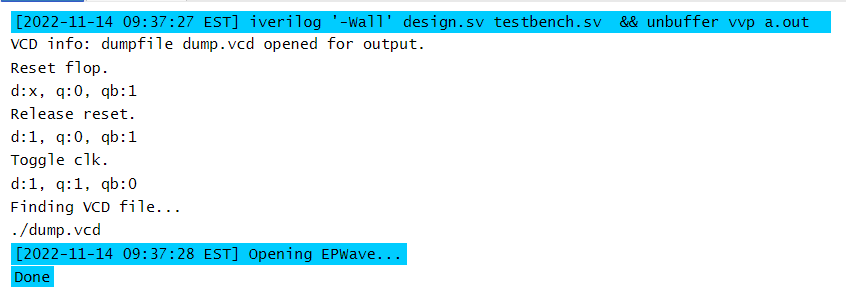
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**Question 3: Write a Verilog code to implement D flip flop and validate the code via a suitable Test bench code.**

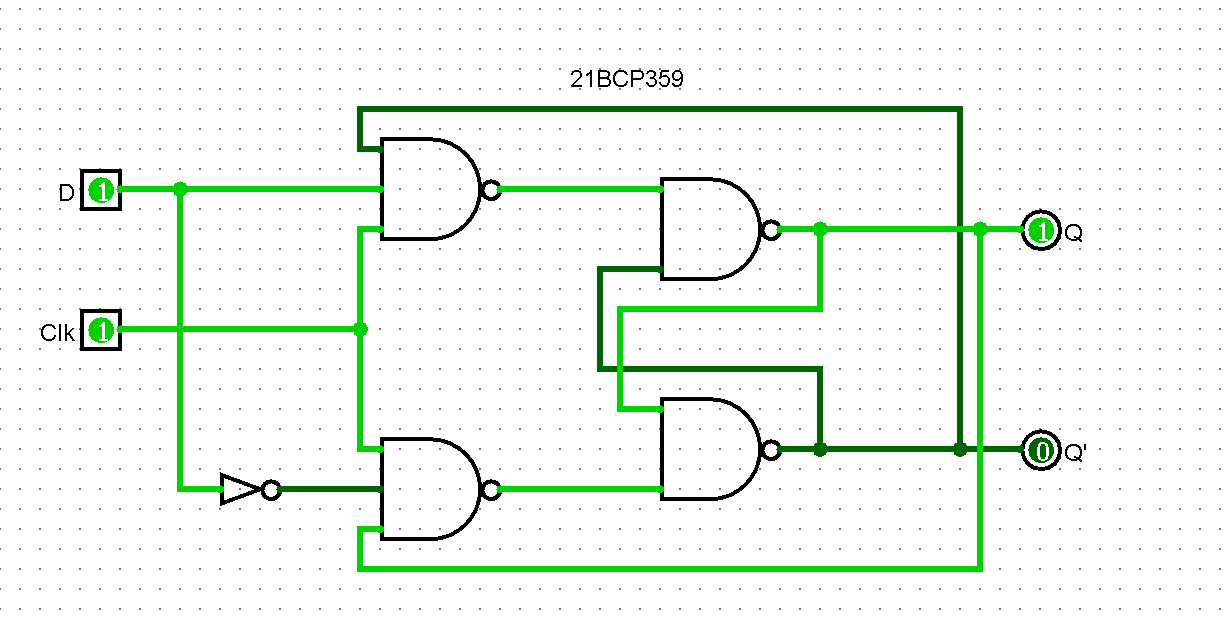
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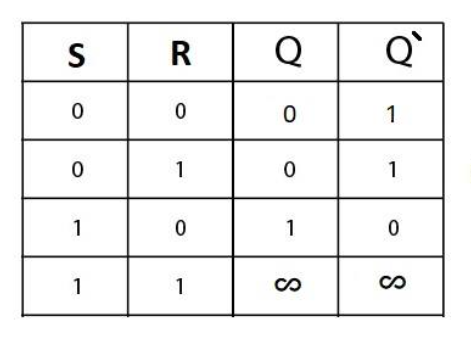
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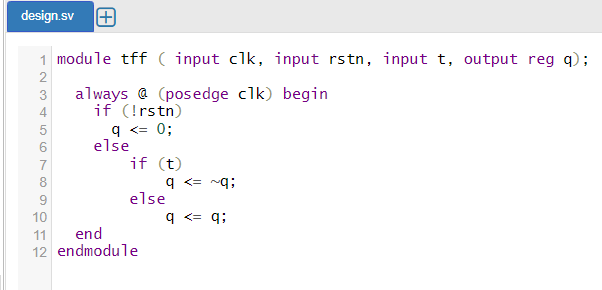
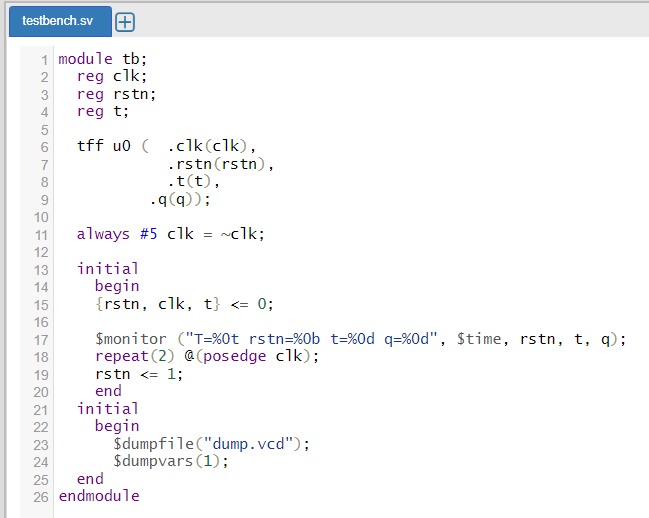
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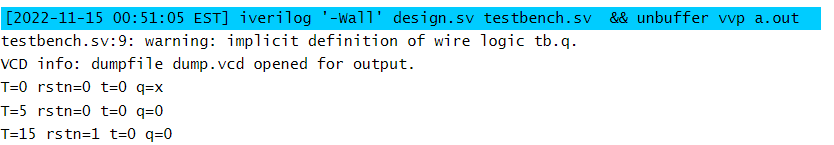
**Question 4: Design a D flip flop in Logisim and validate the circuit.**

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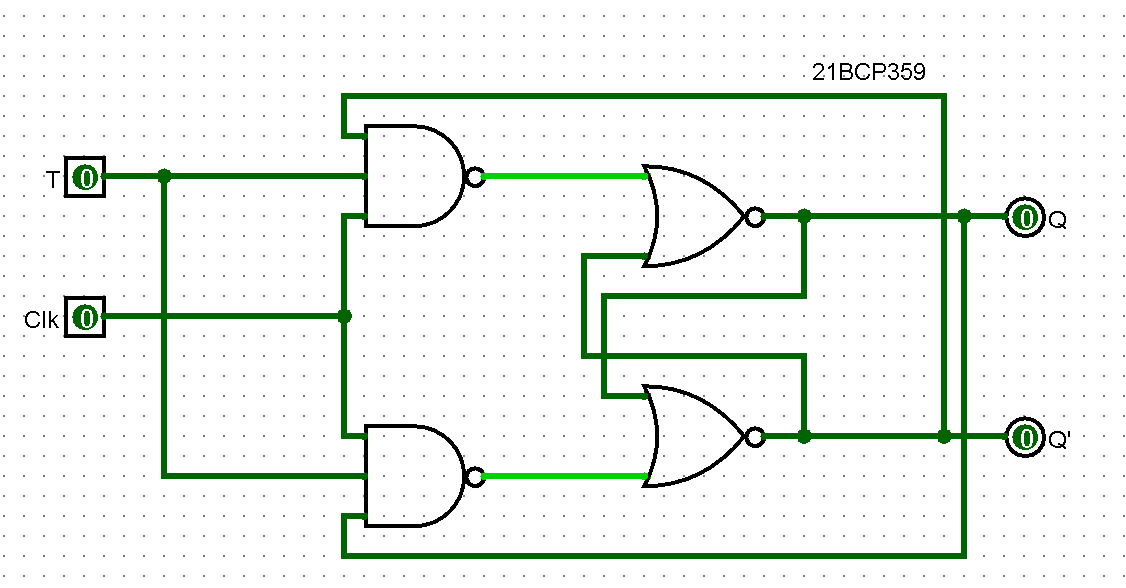
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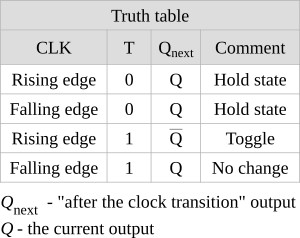
**Question 5: Write a Verilog code to implement T flip flop and validate the code via a suitable Test bench code.**

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**Question 6: Design a T flip flop in Logisim and validate the circuit.**

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